

CLAIMS:

1. A semiconductor arrangement comprising:

- a substrate having a substrate layer (13) with an upper surface and a lower surface, the substrate layer (13) being of a first conductivity type;
- a first buried layer (12) in the substrate, extending along said lower surface below a first portion of said upper surface of said substrate layer (13), and a second buried layer (12) in the substrate, extending along said lower surface below a second portion of said upper surface of said substrate layer (13);
- a first diffusion region (26) in said first portion of said substrate layer (13), being of a second conductivity type opposite to said first conductivity type and having a first distance to said first buried layer (12) for defining a first breakdown voltage between said first diffusion region (26) and said first buried layer (12);
- a second diffusion region (45) in said second portion of said substrate layer (13), being of said second conductivity type and having a second distance to said second buried layer (12) for defining a second breakdown voltage between said second diffusion region (45) and said second buried layer (12);

said first distance being larger than said second distance such that said first breakdown voltage is larger than said second breakdown voltage.

2. The arrangement according to claim 1, wherein said first diffusion region (26) is a base (3) of a bipolar transistor and said first buried layer (12) is a collector (5) of said bipolar transistor.

3. The arrangement according to claim 1 or 2, wherein said second diffusion region (45) is an anode of a protection diode (9) and said second buried layer (12) is a cathode of said protection diode (9).

4. The arrangement according to any of the preceding claims, wherein said first buried layer (12) is connected to said second buried layer (12), and said first and second buried layers (12) are manufactured in the same step.

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5. The arrangement according to any of the preceding claims, further comprising a channel stopper region (42) in said second portion of said substrate layer (13); the channel stopper region (42) being of said first conductivity type, for electrically isolating said second portion of said substrate layer (13) within the substrate (6), wherein said channel stopper region (42) is arranged to extend substantially as an extended channel stopper region (47) in between said second diffusion region (45) and said second buried layer (12), for reducing said second breakdown voltage.

10 6. A method of manufacturing a semiconductor arrangement, comprising the steps of:

- providing a substrate with a substrate layer (13) with an upper surface and a lower surface, the substrate layer (13) being of a first conductivity type, a first buried layer (12) being provided in the substrate, extending along said lower surface below a first portion of said upper surface of said substrate layer (13), and a second buried layer (12) being provided in the substrate, extending along said lower surface below a second portion of said upper surface of said substrate layer (13);
- diffusing a first diffusion region (26) in said first portion of said substrate layer (13), being of a second conductivity type opposite to said first conductivity type and having a first distance to said first buried layer (12) for defining a first breakdown voltage between said first diffusion region (26) and said first buried layer (12);
- diffusing a second diffusion region (45) in said second portion of said substrate layer (13), being of said second conductivity type and having a second distance to said second buried layer (12) for defining a second breakdown voltage between said second diffusion region (26) and said second buried layer (12);

25 said first distance being larger than said second distance such that first breakdown voltage is larger than said second breakdown voltage.

30 7. A method according to claim 6, wherein said first and second diffusion regions (26, 45) are formed by depositing, in a single manufacturing step, a first poly-silicon layer (23) in a first area in said first portion and a second poly-silicon layer (44) in a second area in said second portion, and diffusing said first and second diffusion regions (26, 45) from said first and second poly-silicon layers (23, 44), respectively, in a single annealing step, said first area being smaller than said second area.

Sub Ae > 8. A method according to claims 6-7, further comprising the step of forming by ion-implantation a channel stopper region (42) in said second portion of said substrate layer (13); the channel stopper regions (42) being of said first conductivity type, for electrically isolating said second portion of said substrate layer (13) within the substrate (6) wherein said channel stopper region (42) is formed by ion-implantation as an extended channel stopper region (47) in between said second diffusion region (45) and said second buried layer (12), for reducing said second breakdown voltage.

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